REMARKS

Applicants respectfully request reconsideration of the present application, as amended, and consideration of the following remarks.

Claims 1-19 are pending. The Examiner has rejected claims 1-19. In the accompanying amendment, claims 1-19 have been cancelled, and new claims 20-37 have been added. Support for the amendments to the claims may be found in the specification, the claims, and the drawings, as originally filed. On account of the foregoing support for the new claims, it is respectfully submitted that the new claims do not add new matter.

Rejections Under 35 U.S.C. 102

The Examiner has rejected Claims 1-19 under 35 U.S.C. § 102(b) as being anticipated by Grochowski et al. (U.S. Patent No. 5,535,347) ("Grochowski").

New claim 20 includes the following limitations:

> A method for aligning an instruction stream, the method comprising:
> determining in a length decoder and in a first clock cycle, a length of a current instruction in the instruction stream;
> if the length of the current instruction is less than a predetermined length then shifting the instruction stream to a start of a successive instruction in the instruction stream based on the length of the current instruction, said shifting being performed during the first clock cycle; and
> if the length of the current instruction is greater than the predetermined length then shifting the instruction stream to the start of the successive instruction one clock cycle later.

(claim 20, New)

In the embodiment described on pages 12-15 of the specification, with reference to Figure 5, it may be seen that the output of the length decoder 508 is sent to the shifter 506 which has the capacity to shift 8 bytes of data. The output of the shifter 506 is sent to the length decoder 508 via an intermediate latch. Thus, if the length decoder 508 outputs a length of up to 8 bytes, the shifter 506 shifts to the start of the next instruction in the same clock cycle that the length decoder 508 determined the length of the current instruction.

If, however, the length of the current instruction is greater than 8 bytes, then rotator 508 rotates bytes of the current instruction into the shifter 506 which then sends bytes aligned to the start of the next instruction to the length decoder 508 in the next clock cycle. Thus, if the length of the current instruction is less than a predetermined length (8 bytes in the example above), the instruction stream is shifted to the successive instruction in the same clock cycle in which the length of the current instruction was determined, otherwise if the length of the current instruction is greater than the predetermined length (8 bytes in the example above), then the instructions are shifted to the start of the successive instruction one clock cycle later.

Grochowski discloses a circuit to compute the length of an instruction and to rotate the instruction stream to the beginning of a next instruction based on the length of the instruction (see col. 3, lines 25-45). However, Grochowski fails to teach or suggest that if the length of the current instruction is less than a predetermined number, then the shifting to the start of the successive instruction is performed in the same clock cycle that the length of the current instruction was determined, and if the length of the current instruction is greater than the predetermined length, then the shifting to the start of the successive instruction is performed one clock cycle after the length of the current instruction was determined.

Thus, Grochowski fails to teach or suggest all limitations of claim 20. Accordingly, it is respectfully submitted that claim 20 is not anticipated or rendered obvious by Grochowski.

Given than claims 21-24 depend on claim 20, it is respectfully submitted that these claims are also not anticipated or rendered obvious by Grochowski.

New claim 26 includes the following limitations:

> A method for aligning instructions in an instruction stream, the method comprising:
>
> determining a length of a first instruction in the instruction stream during a length decode stage; and
>
> inputting the length of the first instruction to a two-stage instruction alignment stage comprising first and second shift operations performed by first and second shifters respectively,

wherein an output of the second shift operation comprises instructions of the instruction stream aligned to a start of a successive instruction in the instruction stream immediately following the first instruction, the output of the second shift operation defining an input to the length decode stage, and wherein if the first instruction is contained in the second shifter said first instruction is shifted into a length decoder that performed the length decode stage in the same clock cycle in which the length of the first instruction was determined, and wherein if the first instruction is not contained in the second shifter, said first instruction is shifted from the first shifter one clock cycle later into the length decoder from the first shifter.

(claim 26, new)

Grochowski fails to disclose that if the first instruction is not contained in the second shifter, then the first instruction is shifted from first shifter one clock cycle later into the length decoder.

Accordingly, it is respectfully submitted that Grochowski does not teach or suggest all limitations of claim 26, and that claim 26 is therefore not anticipated or rendered obvious by Grochowski.

Given that claim 27-30 depend on claim 26, it is respectfully submitted that these claims are also not anticipated or rendered obvious by Grochowski.

New claim 31 includes the following limitations:

Logic for aligning instruction in an instruction stream, the logic comprising:
a first shifter;
a second shifter; and
a length decoder, wherein an output of the first shifter forms a direct input to the second shifter, an output of the second shifter is sent to the length decoder via an intermediate latch, and wherein a length of a current instruction in the length decoder is directly input into the second shifter.

(claim 31, new)

Grochowski fails to teach or suggest logic for aligning instruction in a instruction stream, comprising first and second shifters, and a length decoder, wherein an output of

the first shifter forms a direct input to the second shifter, and output of the second shifter is sent to the length decoder via an intermediate latch, and wherein a length of the current instruction in the length coder is directly input into the second shifter.

Accordingly, it is respectfully submitted that claim 31 is not anticipated or rendered obvious by Grochowski. Given that claims 32-34 depend on claim 31, it is respectfully submitted that these claims are also not anticipated or rendered obvious by Grochowski.

New claim 35 includes the following limitations:

> Logic for aligning instructions in an instruction stream, the logic comprising:
>
> first shifting means for shifting bytes of the instruction stream;
>
> second shifting means for shifting bytes of the instruction stream; and
>
> length decoding means for determining a length of an instruction in the instruction stream, wherein an output of the first shifting means forms a direct input to the second shifting means, an output of the second shifting means is sent to the length decoding means via an intermediate latching means, and wherein a length of a current instruction in the length decoding means is directly input into the second shifting means.

(claim 35, new)

Grochowski fails to teach or suggest the limitation of length decoding means for determining the length of an instruction in an instruction stream, wherein an output of the shifting means forms a direct input to the second shifting means, an output of the second shifting means is sent to the length decoding means via an intermediate latching means; and wherein a length of a current instruction in the length decoding means is directly input into the second shifting means. Accordingly, it is respectfully submitted that claim 35 is not anticipated or rendered obvious by Grochowski. Given that 36 and 37 depend on claim 35, it is respectfully submitted that these claims are also not anticipated or rendered obvious by Grochowski.

In conclusion, it is respectfully submitted that all claim objections and rejections have been overcome and that the present application is in condition for allowance, which action is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 02/03/03

Michael J. Mallie
Reg. No. 36,591

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025
(408) 720-8300